CLAIM AMENDMENTS

1. (Currently amended) A multilayer electronic substrate ~~manufactured by~~ comprising:

a first conductor layer and an insulating region arranged on an insulating substrate;

an insulator arranged on said first conductor layer and said insulating region;

second conductor layers arranged on said insulator; and

a resistor ~~arranged on~~ connected electrically between said ~~insulator~~ second conductor layers;

~~and a second conductor layer for sandwiching said resistor to be connected to said resistor; in which~~ wherein an electric characteristic of a circuit is adjusted by trimming said resistor; and

~~is trimmed so as to adjust an electric characteristic of a circuit; wherein: a portion of said first conductor layer, which corresponds to a trimming portion of said resistor, is constituted by an~~ wherein said insulating region is arranged under a part of said resistor in which a trimming portion is disposed.

2. (Currently amended) A multilayer electronic substrate as claimed in ~~claim 1 wherein: said~~ claim 1, wherein a portion of the first conductor ~~layer, which~~ layer which corresponds to the trimming portion ~~of said resistor,~~ is formed by a mask pattern printing operation when said first conductor layer is printed.

3. (Currently amended) A multilayer electronic substrate as claimed in ~~claim 1 wherein: the~~ claim 1, wherein a portion of said first conductor ~~layer, which~~ conductor which corresponds to the trimming portion ~~of said resistor,~~ is formed by a trimming operation after said first conductor layer has been printed ~~in a~~ by solid ~~manner~~ printing.

4. (Currently amended) A multilayer electronic substrate as claimed in ~~claim 1 wherein:~~ claim 1, wherein said insulating region is formed ~~in~~ as an integral body with the insulator ~~arranged between said first conductor layer and said second conductor layer~~.

5. (Currently amended) A multilayer electronic substrate as claimed in ~~claim 1 wherein:~~ claim 1, wherein said insulating region is separately formed ~~with reference to~~ from the insulator ~~arranged between said first conductor layer and said second conductor layer, and is inserted to be arranged~~.

6. (Currently amended) A multilayer electronic substrate as claimed in ~~claim 1 wherein:~~ claim 1, wherein a circuit pattern protection layer ~~is provided in such a manner that said circuit pattern protection layer~~ covers said insulator, said second conductor layer, and said resistor.

7-10. (Canceled)

11. (Currently amended) A multilayer electronic substrate ~~manufactured by~~ comprising:

a first conductor layer and an insulating region arranged on an insulating substrate;

a first insulator arranged on said first conductor layer and said insulating region;

a second conductor layer arranged on said first insulator;

a first resistor ~~arranged on~~ connected electrically with said ~~first insulator~~ second conductor layer;

a second ~~conductor layer for sandwiching said first resistor to be connected to said first resistor; a second~~ insulator arranged on said first insulator, said first resistor, and said second conductor layer;

a second resistor arranged on said second ~~insulator, and~~ insulator;

a third conductor layer for sandwiching said second resistor to be connected to said second resistor; and

a circuit pattern protection layer arranged on said second insulator, said third conductor layer, and said second resistor; ~~wherein:~~

wherein said first resistor is trimmed so as to adjust an electric characteristic of a circuit and said second resistor is trimmed so as to adjust an electric characteristic of a circuit; and

wherein a portion of said first conductor layer, which corresponds to a first trimming portion of said first resistor, is constituted by a first insulating region; and a portion of said first conductor layer, which corresponds to a second

trimming portion of said second resistor, is constituted by a second insulating region.

12. (Currently amended) A multilayer electronic substrate as claimed in ~~claim 11 wherein:~~ claim 11, wherein both the portion of said first conductor ~~layer, which~~ layer which corresponds to the first trimming portion of said first ~~resistor, and~~ resistor and the portion of said second conductor ~~layer, which~~ layer which corresponds to the second trimming portion of said second ~~resistor, are~~ resistor are formed by a mask pattern printing operation when said first conductor layer is printed.

13. (Currently amended) A multilayer electronic substrate as claimed in ~~claim 11 wherein:~~ claim 11, wherein both the portion of said first conductor ~~layer, which~~ layer which corresponds to the first trimming portion of said first ~~resistor, and~~ resistor and the portion of said second conductor ~~layer, which~~ layer which corresponds to the second trimming portion of said second ~~resistor, are~~ resistor are formed by a trimming operation after said first conductor layer has been printed ~~in a~~ by solid printing ~~manner~~.

14. (Currently amended) A multilayer electronic substrate as claimed in ~~claim 11 wherein:~~ claim 11, wherein both said first insulating region and said second insulating region are formed ~~in~~ as an integral body with at least one of the ~~insulator arranged between said first conductor layer 3 and said second~~

~~conductor layer~~ insulators.

15. (Currently amended) A multilayer electronic substrate as claimed in ~~claim 11 wherein:~~ claim 11, wherein both said first insulating region and said second insulating region are separately formed ~~with reference to the insulator arranged between said first conductor layer and said second conductor layer~~.